Are LLM-Generated GPU Kernels Production-Ready? A Trace-Driven Benchmark and Optimization Agent

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Abstract

Existing GPU kernel generation benchmarks draw problems from synthetic or curated sources that diverge from deployed workloads. We present **Atrex-Bench**,[1] a benchmark whose 30 operators and 440 shapes are sampled directly from full-cluster production inference traces of compute-limited, memory-rich GPUs. Each problem carries an importance weight derived from its share of observed GPU time, weighted by application card-hours and computed separately for the serving phases in which it runs, together with a per-problem roofline ceiling, so the aggregate score emphasizes the kernels that consume the most serving time. Evaluating six frontier coding agents on Atrex-Bench shows that even the best vanilla model reaches only $\sim 10\%$ of the hardware roofline on production operators—and correctness alone overstates capability, since much of the apparent pass rate comes from PyTorch fallbacks rather than kernels the model wrote. To close this gap, we co-release **Atrex-Kernel-Agent** (AKA),[2] a profile-driven kernel-optimization agent that combines iterative measure–revise search, optimization dropout for escaping stalled search contexts, and a layered GPU-optimization knowledge base (298 reference-kernel files and 244 optimization-knowledge documents, plus external upstream reference projects for API/ISA lookup). In a controlled case study, the agent converts zero-FlyDSL fallbacks into real kernels that match or exceed hand-tuned production baselines.

1 Introduction

LLM coding agents can now write GPU kernels that compile, pass correctness checks, and approach hand-written performance on simple workloads. A line of benchmarks has tracked this progress, contributing the PyTorch-reference task format, roofline-style scoring against hardware ceilings, multi-vendor targets, and production hot-swapping [Ouyang et al., 2025, Saroufim et al., 2025, Li et al., 2025, Wen et al., 2025, Xing et al., 2026, Zhu et al., 2026, Lin et al., 2026]. The natural next question is whether these agents are ready for *production*: can they write the kernels a real serving stack actually runs, on the hardware that fleet actually deploys, well enough to replace or improve production kernels?

Existing benchmarks cannot answer this, because their problems are synthetic or curated and so diverge from deployed workloads on three axes that decide production value. First, *which shapes*: a production fleet runs a heavily skewed distribution—in our traces, the top five operators carry $\approx 64\%$ of GPU wall-time—that a uniform synthetic grid does not reproduce. Second, *which kernels matter*: an unweighted task average treats a rare elementwise op like a fused-attention path that dominates

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[1] `https://github.com/alibaba/atrex-bench`

[2] `https://github.com/alibaba/atrex-kernel-agent`

latency. Third, *how good is good enough*: a kernel must approach the hardware roofline on its own shape, not merely beat an unoptimized baseline. A benchmark that misses these axes reports scores that do not predict deployability.

The workload axes force a different benchmark contract. The workload source must come from online serving traces rather than a hand-written operator list; the problem weights must preserve production skew rather than average every task equally; and the denominator must be a per-shape hardware ceiling rather than a mutable software baseline. The contract should also hide production provenance and roofline answers during generation; otherwise, an agent can exploit upstream names, known kernels, or the scoring formula instead of solving the kernel.

Atrex-Bench implements this contract. It samples problems from production inference traces on compute-limited, memory-rich GPU fleets spanning XPU-A[3] and H20, with more than 10k deployed accelerators; the current release contains 30 operators and 440 hot shapes drawn from 1,303 profiles and $\sim$20 deployed models across vLLM, SGLang, AITER, and RTP-LLM [Kwon et al., 2023, Zheng et al., 2024, AMD, 2025a, Tan et al., 2026]. It weights each (op, shape) by its serving-time share, scores each against a per-problem roofline ceiling, and hides upstream provenance and roofline artifacts from candidate agents. Evaluating six frontier coding agents exposes a gap that prior benchmarks miss: the best candidate reaches only 10.7% of the reference-derived hardware roofline ($S_{\text{agg}} = 0.107$), and no agent matches the deployed production kernel (§4). We also analyze the generated code after evaluation and identify a form of correctness reward hacking: models can pass by delegating to PyTorch fallbacks while writing little target-DSL code (e.g., Qwen3.7-Max achieves 84.8% correctness with only 43.8% FlyDSL adoption [AMD, 2025b]), so correctness overstates target-DSL use (§4.3).

The residual gap is concentrated in domain knowledge—roofline reasoning, hardware-specific instruction selection, and accumulated tactics—rather than raw coding ability. Motivated by this, we build **Atrex-Kernel-Agent** (AKA), which pairs a profile-driven measure–revise workflow with *optimization dropout*—a partial restart that escapes stalled search contexts—and a layered optimization-knowledge base. In a controlled study AKA mitigates both failure modes: it closes the target-DSL-dominance gap on a weaker model by converting 0%-FlyDSL fallbacks into near-100%-FlyDSL kernels ($6.7\times$ over the fallback on `attention_forward`), and it narrows the residual roofline gap on a stronger one (S $0.28 \rightarrow 0.42$), with kernels that overtake the hand-tuned production baseline on both attention operators (§5).

Contributions. In summary, this work contributes: (1) **Atrex-Bench**, the first kernel-generation benchmark sourced from full-cluster production traces and scored with an importance-weighted, per-problem roofline metric [Williams et al., 2009] (§3); (2) a release contract that packages production-derived references, shape sets, hidden provenance, hidden roofline artifacts, and refreshable importance weights; (3) an evaluation of six frontier coding agents that quantifies how far they remain from deployability—a best $S_{\text{agg}} = 0.107$—and uses post-hoc target-DSL-dominance analysis to expose a measurable correctness illusion (§4); and (4) **AKA**, a profile-driven optimization agent that closes much of this gap, turning fallbacks into real kernels that overtake hand-tuned production baselines (§5). Both artifacts are released as open source.

2 Related Work

2.1 LLM Kernel Generation Benchmarks

KernelBench [Ouyang et al., 2025] pioneered LLM kernel-generation evaluation with a 250-task, three-level difficulty suite drawn from PyTorch reference modules. BackendBench [Saroufim et al., 2025], from the Meta PyTorch team, reframes the problem as "ship a correct & fast backend for PyTorch" and adds a hot-swap path for replacing ATen kernels in place. TritonBench [Li et al., 2025] targets Triton kernels specifically. MultiKernelBench [Wen et al., 2025] extends KernelBench to 285 recategorized tasks and ports the evaluation harness to NVIDIA L20, Huawei Ascend NPU, and Google TPU. FlashInfer-Bench [Xing et al., 2026] establishes a closed-loop framework (Trace schema + leaderboard + dynamic substitution via `apply()`) atop the FlashInfer engine, blurring the line between benchmarking and production hot-swapping. More recently, CUDABench [Zhu et al., 2026] reframes the problem as *text-to-CUDA* (rather than *PyTorch-to-CUDA*) and introduces a roofline-

[3]We use XPU-A as a desensitized name for the non-NVIDIA accelerator evaluated in this paper.

Table 1: Cross-benchmark capability matrix (positioning, not ranking), ordered by release. "Roofline": ships a per-problem roofline/Speed-of-Light bound; "Imp.-wtd.": importance-weighted aggregate; "Prod.-sampled": problems sampled from production traffic.

Benchmark	Source	Roofline	Imp.-wtd.	Prod.-sampled
KernelBench [Ouyang et al., 2025]	synth. PyTorch	✗	✗	✗
BackendBench [Saroufim et al., 2025]	PyTorch ATen + traces	✗	✗	partial
TritonBench [Li et al., 2025]	hand-crafted	✗	✗	✗
MultiKernelBench [Wen et al., 2025]	KernelBench fork	✗	✗	✗
FlashInfer-Bench [Xing et al., 2026]	curated + traces	✗	✗	partial
CUDABench [Zhu et al., 2026]	public CUDA repos	✓	✗	✗
SOL-ExecBench [Lin et al., 2026]	curated	✓	✗	✗
Atrex-Bench	**online production trace**	✓	✓	✓

based score over a 1,500-prompt set sampled from open-source CUDA repositories. NVIDIA's SOL-ExecBench [Lin et al., 2026] targets "Speed-of-Light"-style hardware-utilization measurement.

Atrex-Bench shares the goal of measuring LLM kernel generation and reuses several conventions established above (PyTorch-defined references, three-stage compile/correctness/perf gating, roofline-style scoring); it adds two complementary capabilities visible at a glance in Table 1: it draws its problem set from *online production traces* rather than synthetic or curated tasks, and it scores kernels under an *importance-weighted* aggregate that reflects production time share. We also plan to refresh the problem distribution from production traffic as workloads evolve, so the benchmark can track deployed needs while preserving versioned snapshots for reproducibility.

2.2 Roofline Model and Hardware Performance Bounds

The roofline model [Williams et al., 2009] bounds a kernel's achievable performance by $\min(\mathrm{P_{peak}},\ \mathrm{AI} \cdot \mathrm{B_{peak}})$, giving a hardware-independent utilization metric widely used in GPU performance engineering. CUDABench [Zhu et al., 2026] and SOL-ExecBench [Lin et al., 2026] are the closest prior benchmarks to adopt this metric; Atrex-Bench differs in deriving a versioned roofline ceiling for each production-derived problem and feeding per-kernel roofline achievement into an importance-weighted aggregate rather than a uniform mean.

2.3 Skills and Knowledge Libraries for Code Agents

Equipping an agent with a retrievable skill library has been explored in embodied settings (Voyager [Wang et al., 2023]), general reasoning (Self-Discover [Zhou et al., 2024]), and software engineering (SWE-agent [Yang et al., 2024]; Anthropic Skills [Anthropic, 2025]). Recent GPU-kernel systems bring the same idea into optimization: AKO [Xie et al., 2026] packages existing coding agents in an optimization harness with benchmark/profiler interfaces and closed-loop campaigns, while KDA [MIT HAN Lab, 2026] codifies a CUDA-kernel workflow around task contracts, planning, verification, profiles, and reusable kernel knowledge. AKA differs in two main ways. First, its *optimization dropout* mechanism masks stale iteration memories while preserving the accepted kernel and audit trail, giving a fresh sub-agent enough context to explore a different optimization direction rather than remaining trapped in a local optimum. Second, it uses a layered knowledge base that combines expert-contributed optimization experience and hardware facts with reference kernels and best practices retrieved from upstream open-source projects. Together with official-profiler feedback, these mechanisms turn knowledge retrieval into an iterative search process rather than a one-shot injection of additional context (§5.5).

3 Atrex-Bench: Design

This section describes how Atrex-Bench constructs benchmark operators and shape-level artifacts from production traces (Sections 3.1–3.2), how it derives per-problem roofline bounds and importance weights (Sections 3.3–3.4), how it scores candidate kernels (§3.6), and how it evaluates submitted kernels (§3.7). Figure 1 provides an end-to-end overview of this lifecycle.

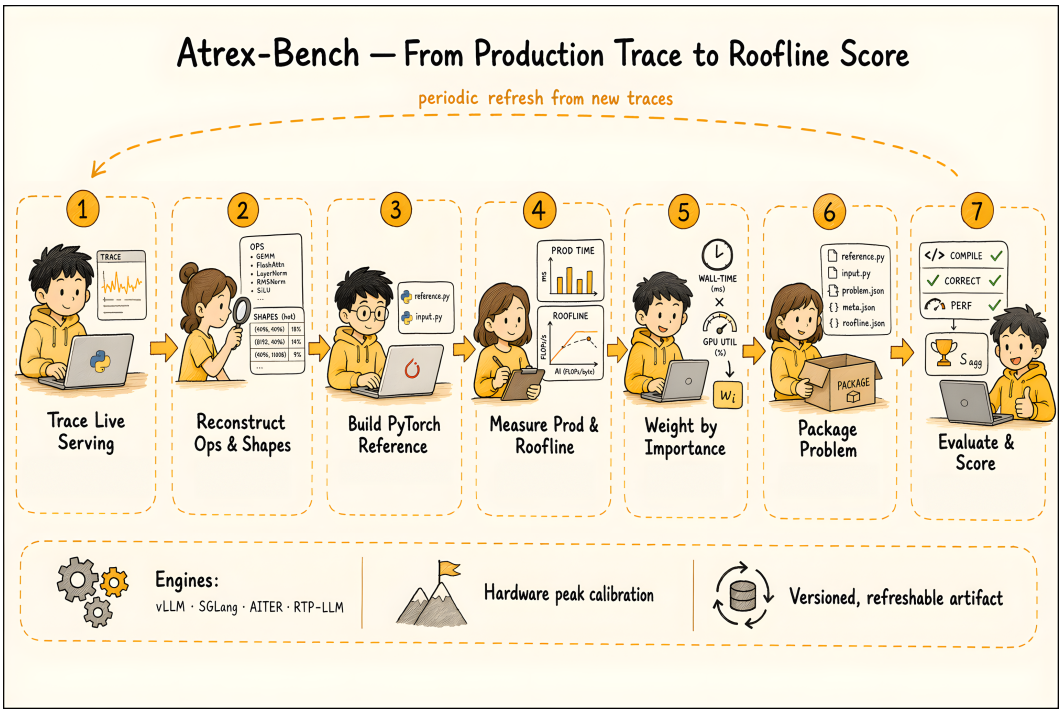

Figure 1: Atrex-Bench lifecycle, from production trace to roofline score: trace live serving, reconstruct operators and shapes, build PyTorch references, derive per-problem roofline bounds and importance weights, package the hidden-provenance problem set, and run the three-stage compile/correctness/performance gate.

3.1 From Production Traces to Operators and Shapes

The benchmark's problem set is sourced from online production traces collected on selected XPU-A and H20 inference clusters with more than 10k deployed accelerators. The tracer attaches to running workloads without relaunching the service or inserting application-level instrumentation. It combines Python-frame context (operator phase, batch/token shape, framework state) with vendor runtime traces (kernel launches, timing, streams, memory operations, and graph anchors), then correlates host and device events through correlation IDs when available and timestamps or graph anchors otherwise. This gives a cross-layer view of which framework operation produced each device kernel and under which serving shape.

From traces to benchmark units. The construction pipeline maps raw kernel records into computation-level operator families rather than framework-specific kernel names, so semantically identical operators from vLLM [Kwon et al., 2023], SGLang [Zheng et al., 2024], AITER [AMD, 2025a], and RTP-LLM [Tan et al., 2026] can share one benchmark problem. Each released (operator, shape) entry retains upstream provenance in `metadata.json` for reproducibility.

Reference and shape construction. For each operator, we reimplement the production logic as a hardware-agnostic PyTorch reference (`reference.py`) and validate it against the production kernel. Shape sets come directly from traced tensor dimensions when available; otherwise, fixed model dimensions are recovered from deployment configuration and dynamic dimensions (e.g., token count, batch size) are set to deployment-typical values. Because raw traces contain many near-duplicate variants, the pipeline keeps architecture-fixed dimensions exact and buckets dynamic token dimensions from single-token decode to long-context prefill. The current release contains **30** operators and **440** representative shapes.

Baselines and weights. For each retained (operator, shape), we record the production framework kernel's observed production runtime as a deployment baseline and a sanity check for the roofline bound. The pipeline also assigns each operator a phase label (`prefill`, `decode`, or `prefill/decode`) and

Table 2: Per-operator problem specification files in Atrex-Bench; "Visible" marks files available to candidate agents during generation.

File	Contents	Visible
`reference.py`	Executable PyTorch specification of the operator semantics.	✓
`input.py`	Input generator for randomized and corner-case tensors.	✓
`shapes.json`	Production-derived shape configurations, including model dimensions and serving-time dynamic dimensions.	✓
`metadata.json`	Release metadata: operator identity, dtype information, production baseline time, and upstream provenance.	✗
`roofline.json`	Scoring metadata: semantic work/traffic estimates and per-hardware speed-of-light time.	✗

derives its importance weight w_i from its share of observed device time, weighted by application card-hours and computed separately for the serving phases in which it runs (§3.4).

3.2 Problem Specification Format

Each Atrex-Bench operator is shipped as a directory containing a fixed five-file contract, summarized in Table 2.

Generation–evaluation boundary. The five-file contract separates the operator specification used for generation from the artifacts used only by the evaluator. During generation, the visible surface is the executable problem statement: `reference.py`, `input.py`, `shapes.json`, and the prompt constraints. For generation CLIs with explicit tool controls, we further restrict the callable tool surface: default runs expose local workspace inspection, search, editing, and shell-based build/test iteration, while web-retrieval, notebook-editing, and delegation and auxiliary-agent tools are excluded from comparable benchmark runs. Optimizer-augmented experiments that intentionally enable these tools are therefore treated as a separate setting. The hidden files provide provenance and scoring state to the evaluator, but are not part of the generation prompt: `metadata.json` contains upstream provenance, and `roofline.json` contains the per-shape scoring denominators. During evaluation, the generated file is imported into a fresh environment that contains the full benchmark state and evaluator, decoupling what the model can read from how its output is judged. This boundary also prevents direct leakage from answer-bearing artifacts, such as recovering the source kernel by name or tuning directly to the roofline denominator. Per-operator importance weights (§3.4) are shipped as a release-level artifact, so that re-weighting on a new trace does not require touching individual problem assets.

3.3 Per-Problem Roofline Bound Derivation

The roofline bound gives a hardware lower bound on the latency of each benchmark unit. We derive it in two steps. First, accelerator compute throughput and memory bandwidth peaks are calibrated once and recorded as release constants. Second, the reference implementation defines the unit's semantic work F_j and memory traffic M_j. For a target accelerator with dtype-specific compute peak P_{τ_j} and memory bandwidth β, the speed-of-light latency for unit j is

$$T_{\text{roofline},j} = \max\left(\frac{F_j}{P_{\tau_j}}, \frac{M_j}{\beta}\right). \tag{1}$$

This $T_{\text{roofline},j}$ is stored in `roofline.json` and serves as the per-problem denominator in the roofline achievement score (§3.6).

3.4 Importance Weighting

Each operator is assigned an importance weight.

Importance weight w_i. The weight estimates an operator's share of production GPU time while preserving both the deployed application mix and the prefill/decode distinction. Let a index applications and let p_a be application a's fraction of fleet card-hours, with $\sum_a p_a = 1$. Operator i may comprise multiple device kernels. If kernel r is invoked $m_{a,\phi,r}$ times in application a during phase

Table 3: Top-10 Atrex-Bench operators by importance weight w_i (Equation 3). "Score" is the normalized app-card-hour-weighted, phase-aware GPU-time share; "Shapes" the number of shipped (init/input) configurations; "Dtype" the operator's primary precision.

Operator	Score w_i	Cum.	Shapes	Dtype
`unified_attention`	0.361	0.361	25	bf16
`fused_moe`	0.104	0.465	23	bf16
`block_scaled_mm`	0.085	0.550	24	fp8_e4m3
`fp8_blockscale_fused_moe`	0.047	0.596	6	fp8_e4m3
`paged_attention_decode`	0.040	0.637	8	bf16
`reshape_and_cache`	0.040	0.677	8	bf16
`topk_filter`	0.032	0.709	8	fp32
`gated_delta_rule_update`	0.032	0.741	17	bf16
`fused_qkv_rope`	0.031	0.771	6	fp16
`rms_norm`	0.025	0.796	56	bf16
20 tail operators (combined)	0.204	1.000	259	mixed

$\phi \in \{\text{prefill}, \text{decode}\}$, and invocation ℓ has duration $d_{a,\phi,r,\ell}$, its cumulative observed device time is

$$D^{\phi}_{i,a} = \sum_{r \in \mathcal{K}_i} \sum_{\ell=1}^{m_{a,\phi,r}} d_{a,\phi,r,\ell}, \qquad D^{\phi}_{a} = \sum_{j} D^{\phi}_{j,a}. \tag{2}$$

The ratio $D^{\phi}_{i,a}/D^{\phi}_{a}$ is therefore the fraction of observed GPU time consumed by operator i within that application's collection window for phase ϕ; invocation frequency is represented by the sum over $m_{a,\phi,r}$. Let Φ_i denote the phases in which operator i runs. We use the single phase share for a prefill-only or decode-only operator and the simple average of the two phase shares for an operator that runs in both phases. Weighting this quantity by the application's fleet card-hour share gives

$$\tilde{w}_i = \sum_{a} p_a \, \frac{1}{|\Phi_i|} \sum_{\phi \in \Phi_i} \frac{D^{\phi}_{i,a}}{D^{\phi}_{a}}, \qquad w_i = \frac{\tilde{w}_i}{\sum_j \tilde{w}_j}, \qquad \textstyle\sum_i w_i = 1. \tag{3}$$

The final normalization restricts the distribution to the operators retained in the benchmark release. The current release aggregates **1,303** production profiles spanning four serving frameworks (vLLM, SGLang, AITER, and RTP-LLM), and the weight distribution is heavily skewed: the top five operators carry $\approx$**64%** of the weight (`unified_attention` 36.1%, `fused_moe` 10.4%, `block_scaled_mm` 8.5%, `fp8_blockscale_fused_moe` 4.7%, `paged_attention_decode` 4.0%), while the remaining 25 operators share the rest. These weights are recomputed from production traces whenever the benchmark distribution is refreshed.

Equation 3 is what makes the aggregate *production-weighted* rather than suite-uniform: an operator that dominates deployed wall-time dominates the score, however many or few shapes it contributes.

3.5 Operator and Shape Distribution

The current release covers **30** production operators with **440** hot shapes in total. Several structural properties of the resulting distribution are worth surfacing because they shape what the benchmark actually measures.

Heavy-tailed importance. Importance weights are concentrated in a small number of operators rather than spread evenly. Table 3 reports the ten operators with the largest app-card-hour-weighted, phase-aware GPU-time shares: the top five (`unified_attention`, `fused_moe`, `block_scaled_mm`, `fp8_blockscale_fused_moe`, `paged_attention_decode`) together account for roughly $\mathbf{64}\%$ of the normalized production importance, and the top ten for roughly $\mathbf{80}\%$. The remaining 20 operators each contribute under 3% but still cover several distinct families (RoPE, RMS-norm variants, MoE-gating utilities, paged-cache management, fp8 dynamic quantization, top-k filtering). The aggregate score in §3.6 therefore rewards making the head right while still requiring correctness on the long tail.

Mixed precision is the norm. The 30 operators span five distinct precisions—bf16 (19 operators), fp8_e4m3 (5), fp16 (2), fp32 (2), and int32 (2). Operators that look superficially similar can

ship at different precisions: `fused_moe` runs in bf16 while `fp8_blockscale_fused_moe` runs in fp8_e4m3, and `block_scaled_mm` uses fp8_e4m3 throughout. Two consequences flow from this for the methodology: hardware peaks P_{peak} must be parameterized per-dtype (§3.3), and a candidate kernel cannot achieve a high roofline score by silently up-casting to a more peak-favorable dtype, because the correctness gate (§3.7) compares against the reference at its declared dtype.

Shape count is decoupled from importance. The number of shapes per operator (column "Shapes" in Table 3) reflects the operator's *shape diversity* in production, not its importance. `rms_norm` ships 56 shapes but carries only 2.5% of the weight; `paged_attention_decode` ships 8 shapes but carries 4.0%. This decoupling is why the aggregate is weighted by w_i rather than by raw $(\text{op}, \text{shape})$ count: a candidate that aces 50 rms-norm variants and fails attention should not outrank one that does the reverse.

Compute- vs. memory-bound regime. The (operator, shape) pairs span a wide range of arithmetic intensity (AI = FLOPs / bytes moved), and the regime depends on both the operator and the shape: a GEMM-based operator like `fused_moe` is memory-bound at single-token decode but compute-bound at large-batch prefill. Across the 440 shapes, the compute-bound end is dominated by large-batch GEMM and attention shapes (AI > 100), while normalization and activation shapes (`rms_norm`, `silu_and_mul`; AI < 1) are bandwidth-limited regardless of token count, and pure data-movement operators (`reshape_and_cache`, `topk_filter`) perform no arithmetic at all. The absolute scale varies accordingly: a single large-batch `fp8_blockscale_fused_moe` shape performs $\sim$400B FLOPs over $\sim$7 GB, while a single-token `fused_qkv_rope` shape performs $\sim$15K FLOPs over $\sim$29 KB—seven orders of magnitude in both dimensions. The benchmark thus exercises both regimes across representative token lengths—a property that proves diagnostic in §4.5, where agents reach several times more of the roof on memory-bound shapes than on compute-bound ones.

Production model and provenance coverage. The 440 shapes are drawn from $\sim$20 production-model deployments spanning MoE architectures (e.g., Qwen3 MoE variants and DeepSeek-R1), vision–language models (Qwen3-VL), and dense models (QwQ-32B, Qwen3-32B, and Qwen3-8B). Because the open-source metadata redacts exact model identities, the public corpus exposes this diversity through operator provenance: assigning each mixed-origin operator to its primary upstream framework, the 440 shapes break down into vLLM (292), SGLang (90), RTP-LLM (38), and AITER (20). The same metadata also records the production baseline backend used for XPU-A measurement, which is AITER for 266 shapes, SGLang for 151, and RTP-LLM for 23. This skew reflects the deployment mix on the traced cluster rather than an artificial balance; the benchmark therefore captures a shared operator vocabulary across a heterogeneous production fleet, not a single model's kernel mix.

3.6 Roofline Score

A candidate is scored at three levels—per shape, per operator, and as a single production-weighted aggregate—so that the headline number reflects kernel-generation ability *as it would be felt in the serving environment*, not average competence over a suite where every operator counts equally.

Per-shape achievement. For an evaluation unit $j = (i, s)$ (operator i, shape s) that passes correctness, with measured candidate time $T_{\text{cand},j}$ and per-shape roofline (speed-of-light) time $T_{\text{roofline},j}$ (§3.3),

$$S_j = \frac{T_{\text{roofline},j}}{T_{\text{cand},j}} \in (0, 1]. \tag{4}$$

T_{roofline} is a hardware lower bound, so a value above 1 indicates inconsistent units, measurement error, or an invalid bound and is treated as an evaluation error rather than clipped. $T_{\text{roofline},j}$ is derived from the *reference* semantics, never from the candidate's own profile, and is fixed across candidates. S_j is left undefined when the unit fails to compile or to match the reference.

Per-operator achievement. Because shape counts vary widely across operators (3 to 56 in the current release), we summarize each operator by the median over its correct shapes, and assign zero where the candidate produces no correct kernel at all:

$$S_i = \begin{cases} \text{median}\{\, S_j : j = (i, s) \text{ correct} \,\}, & \text{operator } i \text{ has a correct shape,} \\ 0, & \text{otherwise.} \end{cases} \tag{5}$$

The zero is deliberate: an operator for which no correct kernel is generated delivers no production value and must not be silently dropped from the aggregate.

Importance-weighted roofline score. The headline metric weights each operator's achievement by its production importance w_i (Equation 3):

$$S_{\text{agg}} = \sum_i w_i \, S_i \ \in [0, 1]. \tag{6}$$

S_{agg} is the production-importance-weighted fraction of the hardware roofline the candidate attains. It is high only when a candidate generates fast, correct kernels for the operators that dominate deployed wall-time: acing a rare operator barely moves it, while failing a heavy one—which enters as $S_i = 0$—costs its full weight. This is what lets S_{agg} measure real-environment kernel-generation ability. We use the weighted arithmetic mean rather than a geometric mean, since the latter collapses to 0 on a single failed operator ($S_i = 0$) and erases all other signal. Operationally, the evaluator first computes the per-shape score S_j for each correct unit, summarizes each operator by the median of its correct shapes (or 0 if none pass), and then applies the production weights in Equation 6.

3.7 Evaluation Procedure

Beyond this separation boundary, each submitted kernel is evaluated through a three-stage gate: (1) *compile*, (2) *correctness*—compared against `reference.py` on randomized and corner-case inputs using the evaluator's numerical-equivalence check, and (3) *performance*—measured in a controlled sandbox with an explicit frequency-lock check, per-iteration L2 flush, and per-shape subprocess isolation. The evaluator returns the candidate's per-shape wall-clock latency $T_{\text{cand},j}$. Only kernels that reach stage (3) contribute to S_j.

With the benchmark design in place, §4 turns to the empirical question that motivates the rest of the paper: how do current LLM agents perform on Atrex-Bench, and where do they fall short?

4 Evaluating Frontier Agents on Atrex-Bench

We run Atrex-Bench on a panel of frontier coding agents, both to report where today's models stand and to test whether the benchmark separates systems that coarser measures rank as equal. Relative-speedup benchmarks lose this resolving power on production serving stacks: once a model learns to call an optimized library, it can pass without writing a kernel at all. We therefore measure at the granularity of a single (op, shape) unit and ask where each generated kernel stops behaving like a deployable one—at compilation, at numerical correctness, at target-DSL dominance, or at the hardware roof.

4.1 Setup

Operators and shapes. The current Atrex-Bench release covers **30** production operators, with **440** hot shapes in total; one full evaluation pass therefore covers 440 (op, shape) pairs. Correctness is checked against the eager reference over $K = 5$ random seeds with tolerances atol $= 10^{-2}$, rtol $= 5 \times 10^{-2}$; a shape counts as correct only when all five seeds pass. Performance is the median end-to-end forward time after warmup. Operators carry very different shape counts (from 3 to 56 each), so every aggregate below is *operator-balanced*: each operator is first summarized over its own shapes and then weighted equally, so a high-shape-count operator does not dominate the score.

Hardware. The experiments in this section are conducted primarily on XPU-A.

Target DSL and agent runtime. We deliberately target **FlyDSL**, a DSL essentially absent from the models' pre-training corpora, so the benchmark tests *learning* rather than recall: a candidate must acquire an unfamiliar programming model from the provided references and follow its constraints precisely, jointly probing in-context learning, instruction-following, and code generation. (The prompt framework also supports Triton, Gluon, and CuteDSL; we leave those to future releases.) Every candidate receives the same prompt and tool set, and the runtime is held fixed—Claude Code, except GPT-5.5 on its native Codex runtime—so the comparison reflects base-model capability rather than harness differences.

Candidates. We evaluate six frontier coding agents—Claude Opus 4.7, GPT-5.5, Qwen3.7-Max, Kimi-K2.6, GLM-5.1, and DeepSeek-V4-Pro—on the full set of 30 operators and 440 units.

Reference baselines. Two non-LLM reference points anchor the "vs" columns. The first is `torch.compile` applied to the reference implementation. The second is the deployed production kernel for each operator (AITER / vLLM / SGLang / RTP-LLM), whose per-shape time is recorded in `metadata.json`. These are reference baselines, not candidates, and appear only in the "vs" columns of Table 4.

Metrics. Each metric first summarizes an operator over its shapes, then aggregates across the 30 operators. Bounded rates use the operator *mean*; the heavy-tailed time ratios use the operator *median*, so a single outlier operator cannot dominate the aggregate.

- *Compile rate*: the mean across operators of (compiled shapes / shapes). A shape compiles only when it produces a completed ahead-of-time MLIR artifact, not merely a module that imports.
- *Correctness*: the mean across operators of (correct shapes / shapes), where a shape is correct iff it compiles *and* matches the eager reference on all $K{=}5$ seeds; compile failures therefore count as incorrect.
- *FlyDSL adoption*: the mean across operators of each operator's mean per-shape FlyDSL device-time share—the fraction of forward-pass device time spent inside `@flydsl.kernel`—which distinguishes target-DSL-dominant execution from paths that delegate primarily to PyTorch or precompiled vendor operators.
- *Roofline achievement* S_{agg}: per shape, $S_j = T_{\text{SOL},j}/T_{\text{cand},j}$, with T_{SOL} derived from the *reference* semantics (§3.3) and fixed across candidates; values above 1 indicate an evaluation error rather than being clipped. Per operator, S_i is the median over its correct shapes (0 if none). The reported headline is the *importance-weighted* aggregate $S_{\text{agg}} = \sum_i w_i S_i$ (§3.6), weighting each operator by its production wall-time share w_i so the score reflects ability where production time actually goes.
- *Reference ratios* $T_{\text{torch.compile}}/T_{\text{cand}}$ and $T_{\text{prod}}/T_{\text{cand}}$, reported as the operator median of per-operator medians over correct shapes (not importance-weighted); a value >1 means the candidate is faster than the baseline.

Compile rate and correctness average over all 30 operators, so an operator a model fails entirely contributes 0. FlyDSL adoption, S, and the ratios are taken only over the operators where they are defined (an operator with no running or no correct shape is excluded, not scored 0); S and the ratios are thus conditioned on each model's own correct operators and read as within-model summaries. The failure-penalizing, production-weighted counterpart is the importance-weighted aggregate S_{agg} of §3.6.

4.2 Main Results

The evaluation gates separate the field before performance is considered. Compile rate ranges from 60.9% to 100%, while correctness and target-DSL adoption widen the separation further (Table 4); §4.7 analyzes where these failures arise.

Correctness and FlyDSL adoption carry most of the remaining separation. Correctness spans roughly forty-five points, from Opus 4.7 at 92.0% down to GLM-5.1 at 46.2%, and FlyDSL adoption splits the field again: Opus 4.7 and GPT-5.5 spend 78.5% and 71.6% of their device time in FlyDSL, but the other four sit below 44%—Qwen3.7-Max, for instance, reaches 84.8% correctness with only 43.8% FlyDSL adoption, a gap we examine in §4.3.

The deployment-facing score reorders the leaders. GPT-5.5 leads on both roofline aggregations, and the gap widens under importance weighting. By the unweighted operator median it edges Opus 4.7 (0.129 vs. 0.104); the importance-weighted S_{agg}, which credits each operator in proportion to its production wall-time share (§3.6), puts it well ahead (0.107 vs. 0.059, roughly $1.8\times$). The widening localizes Opus's weakness: it reaches the roof on the typical, mostly bandwidth-bound operator but falls far short on the production-heavy compute-bound operators that S_{agg} up-weights, where its median achievement is 0.009 against GPT-5.5's 0.074 (§4.5). On the production-weighted score,

Table 4: Main results on XPU-A; all metrics are operator-balanced over the 30 operators. S_{agg} is the importance-weighted roofline achievement (§3.6); the "vs" columns are per-operator medians against `torch.compile` (`t.c.`) and the production kernel.

	Pass rate (%)			Roofline	vs. baseline (×)	
Model	Compile	Correct	FlyDSL	S_{agg}	`t.c.`	prod
Claude Opus 4.7	99.6	**92.0**	**78.5**	0.059	2.29	**0.99**
GPT-5.5	**100.0**	91.1	71.6	**0.107**	**3.06**	0.85
Qwen3.7-Max	97.1	84.8	43.8	0.047	1.10	0.19
Kimi-K2.6	91.5	81.5	40.1	0.043	0.94	0.33
GLM-5.1	60.9	46.2	38.6	0.015	0.97	0.33
DeepSeek-V4-Pro	81.0	62.3	36.4	0.012	0.63	0.12

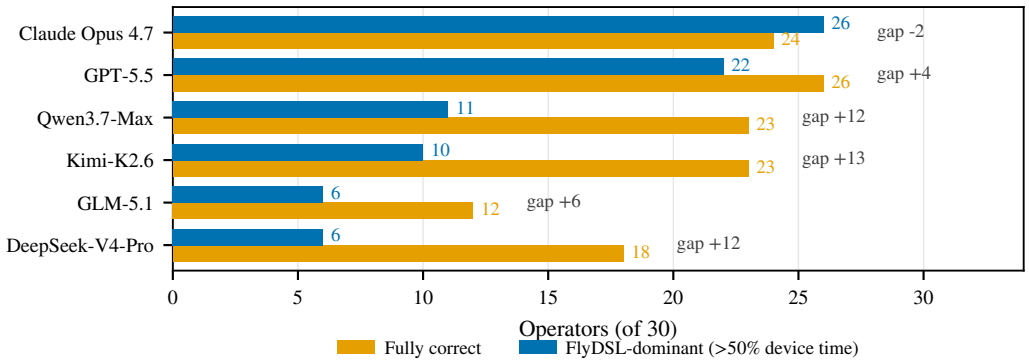

Figure 2: Correctness versus target-DSL dominance per candidate: operators that are fully correct (orange) versus those whose device time is FlyDSL-dominant (blue, $>50\%$); the gap is correctness carried by non-DSL fallbacks.

then, GPT-5.5 is the most hardware-efficient, while Opus 4.7's marginal edge in raw correctness (92.0%) does not carry to the roof where production time concentrates. The absolute numbers stay low: only Opus 4.7 and GPT-5.5 beat `torch.compile` on the median operator ($2.29\times$ and $3.06\times$; Qwen3.7-Max is marginal at $1.10\times$), and *no* candidate beats the deployed production kernel—Opus 4.7 comes closest at $0.99\times$, GPT-5.5 reaches $0.85\times$, and the rest trail to $0.12\times$. Even the best candidate reaches only 10.7% of the reference-derived hardware roofline ($S_{\text{agg}} = 0.107$): passing correctness on production operators does not imply production performance.

4.3 The Correctness Illusion

A passing kernel is not necessarily a written kernel. Because the compile gate admits PyTorch fallbacks and calls into precompiled vendor kernels, a model can accumulate correctness while producing little FlyDSL, and correctness alone then overstates target-DSL use. Counting, per model, the operators that are fully correct against those whose device time is genuinely dominated ($> 50\%$) by FlyDSL exposes the gap (Figure 2). It is widest for the middle of the field: Kimi-K2.6 (23 correct, 10 FlyDSL-dominant), Qwen3.7-Max (23 and 11), and DeepSeek-V4-Pro (18 and 6) all carry roughly half their correct operators on non-DSL paths—answering attention with `scaled_dot_product_attention` and GEMM with a precompiled AITER entry point. Opus 4.7 is the exception, with a *negative* gap (24 correct, 26 FlyDSL-dominant): it writes FlyDSL-dominant kernels on more operators than it fully passes, the signature of target-DSL dominance rather than fallback. The gap is the measurable footprint of specification shortcutting, whose mechanism we revisit in §4.7.

Table 5: Operator difficulty: mean shape-pass rate across the six models (hardest operators shown; the easiest nine pass on all).

Operator (hardest first)	Pass (%)
`fp8_blockscale_fused_moe`	22.2
`fused_rmsnorm_quant`	34.8
`per_token_group_quant_fp8`	44.7
`attention_forward`	45.2
`block_scaled_mm`	56.9
easiest 9 operators	100.0

Table 6: Generation volume vs. quality (§4.6): output tokens, correct operators, and tokens per correct operator.

Cand.	Out (M)	Corr.	Tok/op (K)
Claude Opus 4.7	5.67	24	236
GPT-5.5	1.19	26	**46**
Qwen3.7-Max	2.02	23	88
Kimi-K2.6	2.75	23	120
GLM-5.1	1.84	12	153
DeepSeek-V4-Pro	6.56	18	365

4.4 Hardness Is a Property of the Operator, Not the Model

Averaging each operator's shape-level pass rate across the evaluated models separates operator difficulty from model skill, yielding a ranking that no single model's results would reveal (Table 5). The two ends are far apart: nine operators are solved by every model, while the hardest, `fp8_blockscale_fused_moe`, clears only 22.2% of attempts. The hardest cluster is not random—`fp8_blockscale_fused_moe` (22.2%), `fused_rmsnorm_quant` (34.8%), `per_token_group_quant_fp8` (44.7%), and `block_scaled_mm` (56.9%) are all low-precision quantization fused with a second operation, marking a shared capability frontier rather than a weakness specific to any one model and pointing data curation at fused fp8 kernels. `attention_forward` (45.2%) joins them from the other direction, as the compute-bound case whose roof demands matrix-engine scheduling (§4.5). No operator is failed by every model, so the frontier is hard but not yet out of reach.

The full 30-operator ranking, with production importance weights and per-operator achievement, is in Appendix A (Table 9).

4.5 Where Utilization Goes: Memory- vs. Compute-Bound

Splitting operators by their semantic arithmetic intensity ($\text{AI} = W_{\text{flops}}/Q_{\text{bytes}}$, reference-derived, with a 10 FLOP/byte cut and the per-operator AI defined as the median across its shapes) gives 16 memory-bound and 10 compute-bound operators (four pure-indexing operators with no arithmetic are excluded), and the two regimes behave differently (Figure 3). Every backend reaches a far larger fraction of the roof when the operator is bandwidth-bound, where a correct memory-saturating kernel is comparatively easy to write, than when it is compute-bound and demands tiling and software pipelining. The gap is starkest for Opus 4.7, whose memory-bound median (0.207) is over twenty times its compute-bound median (0.009); GPT-5.5 is the only model to reach a meaningful compute-bound fraction (0.074), and that single difference is what lifts it above Opus 4.7 on the production-weighted S_{agg}, since the heaviest operators are compute-bound. The remaining backends sit far lower in both regimes.

The per-operator scores make the split concrete. On a bandwidth-bound reduction such as `moe_sum_reduce`, Opus 4.7 reaches about three-fifths of the memory roof ($S \approx 0.59$); across the compute-bound operators its median collapses to 0.009, whereas GPT-5.5 holds a non-trivial fraction there (median 0.074, e.g. 0.22 on the fused MoE GEMM). The same ordering holds for most backends, which suggests the bottleneck is not correctness but scheduling: the agents can saturate bandwidth but not the matrix engines. Figure 3 shows this directly—for every model the memory-bound median towers over its compute-bound median, and only GPT-5.5 lifts a compute-bound bar off the floor. The reading is consistent across the panel: agents have learned bandwidth optimization more thoroughly than compute scheduling, and it argues for curating compute-bound, tile-and-pipeline kernels.

4.6 Generation Volume Does Not Predict Quality

Generation volume—the output tokens an agent emits to reach its final candidate—does not predict quality (Table 6). The two heaviest generators land at opposite ends: DeepSeek-V4-Pro emits the most output (6.56M tokens) yet is correct on only 18 operators, whereas Opus 4.7 emits nearly as

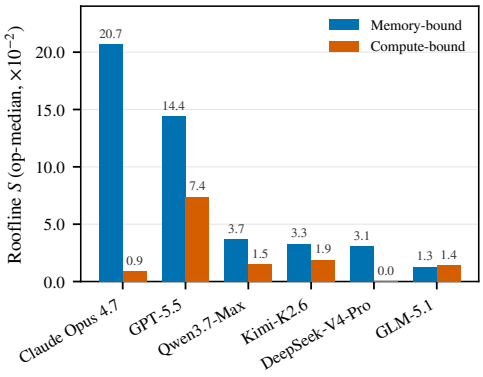

Figure 3: Per-model roofline achievement S by regime (memory- vs. compute-bound operators; S from Equation 5).

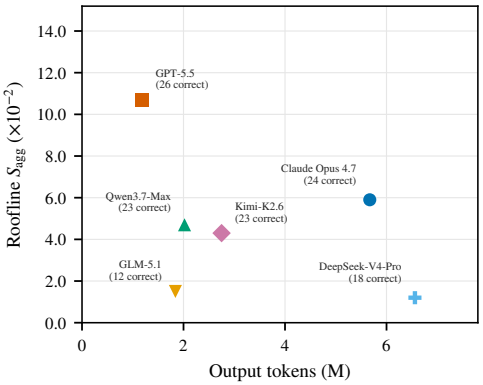

Figure 4: Output-token volume vs. production-weighted achievement S_{agg} per model (labels give fully-correct operator counts).

much (5.67M) and turns it into 24 correct operators and the most DSL-native kernels. The two lightest split the same way: GPT-5.5 reaches the most correct operators (26) on the fewest tokens (1.19M, 46K per correct operator), while GLM-5.1, on a comparable budget (1.84M), produces the fewest (12). More generation implies neither a written kernel nor a correct one. Figure 4 plots the two axes against each other—output-token volume against the production-weighted achievement S_{agg}—and finds no relationship: the lightest generator tops the panel while the heaviest sits near the bottom.

4.7 Error Modes and the Anti-Hacking Contract

Classifying every failing unit across the evaluated models—683 in total—shows both how generated kernels break and what the evaluation contract keeps out.

Compilation does fail, and it concentrates in the weaker backends. The per-shape gate isolates 365 units (53.4% of all failures) that never produce a compiled artifact (Table 7)—failures an import-level gate would pass through to correctness. They track generation quality: GLM-5.1 and DeepSeek-V4-Pro compile only 60.9% and 81.0% of shapes, against 100% for GPT-5.5 (Table 4), with GLM-5.1 alone accounting for 232 of the 365. The failures span the pipeline: syntax-invalid candidates, exceptions on the first forward, ahead-of-time MLIR compilation that exceeds its time budget, and structurally broken modules.

Most surviving failures are silent. Among kernels that do compile, numeric mismatch is by far the most common failure mode (257 units, 37.6% of all failures): the kernel runs and returns a tensor of the right shape and dtype but computes the wrong values. This is the regime only a multi-seed numerical check can catch; a compile-or-run gate would pass it. The remaining runtime failures are a tail of kernels that exceed the execution timeout or raise an exception after a successful compile, alongside 24 correct-but-slow kernels that exceed the performance budget.

Hacking is prevented by construction, and what remains is made visible. The generation workspace never sees `metadata.json` (upstream symbol, provenance, and production timing) or `roofline.json` (the SOL and W/Q bounds), so a model can neither retrieve the reference implementation by name nor fit its output to a scoring formula it is never shown. What this isolation leaves available is specification shortcutting—satisfying the PyTorch reference with a semantically equivalent but non-DSL implementation—and the FlyDSL-adoption metric is what turns that from an invisible pass into a recorded number. The three recurring patterns are PyTorch fallback (e.g. `scaled_dot_product_attention` for attention), precompiled vendor-kernel calls (e.g. AITER GEMM and MoE entry points), and DSL substitution (a Triton kernel where FlyDSL was the target). The correctness illusion of §4.3 is the aggregate of exactly these patterns: high correctness paired with low FlyDSL adoption is the signature of a model optimizing for the reference's input–output

Table 7: Failure taxonomy over all 683 failing units across the six candidates, grouped into compile, runtime, and performance stages.

Failure category	What it is	Count	%
Compile	no compiled artifact produced	365	53.4
exception before first output	raised on import or first forward	261	38.2
compile timeout / OOM-kill	over the AOT compile budget	85	12.4
`Model` not `nn.Module`	not a valid `nn.Module`	19	2.8
Runtime	kernel ran, then failed	294	43.0
numeric mismatch	right shape and dtype, wrong values	257	37.6
runtime timeout	exceeded the execution budget	26	3.8
candidate-raised exception	error after a clean compile	11	1.6
Performance	over the time budget	24	3.5
correct-but-slow timeout	passed numerics, too slow	24	3.5

behavior rather than for writing the kernel. The per-model breakdown of all failure modes is in Appendix A (Table 10).

Takeaway. Across candidates the empirical picture is consistent: vanilla agents, even frontier models, leave substantial production-weighted roofline performance on the table. Some failures are hard—compilation that times out or crashes, numerically wrong output—but the dominant soft failures are kernels that are correct yet reach less than an eighth of the production-weighted roof, and kernels that pass without writing the target DSL at all. The soft failures point less at raw coding ability than at optimization knowledge that exists in expert practice but has not been distilled into a form a base model can retrieve at generation time: tiling strategies matched to a kernel's arithmetic intensity, vendor-specific memory-access patterns, and dtype-aware fusion recipes. Closing that gap without per-task retraining, by making that knowledge retrievable rather than relearned, is the question the next section takes up.

5 Atrex-Kernel-Agent (AKA)

5.1 Motivation

§4.7 leaves two gaps that a stronger base model alone does not close. The first is the *correctness illusion*: a model can satisfy the reference without writing the target DSL, passing while it spends almost no time in FlyDSL (§4.3). The second is the residual roofline gap: kernels with FlyDSL-dominant execution still reach only a fraction of the hardware roof. Both trace to missing GPU-optimization knowledge—roofline reasoning, hardware-specific instruction choices, tiling, and accumulated tactics that frontier models have seen only sparsely in training. AKA addresses both gaps by combining a profile-driven optimization workflow with a curated GPU-optimization knowledge base (GPU Wiki) that the workflow consults at each iteration. Two principles run through the design: every hardware-spec value is sourced from GPU Wiki and archived with its citation (no fabricated specs), and every kernel change is justified by evidence from an official profiler rather than by intuition.

5.2 Architecture and Workflow

AKA is not a single prompt template; it is a routed workflow whose intermediate states are materialized as structured artifacts, profiles, and memory records (Figure 5). The design separates *setup*, *kernel authoring*, *profile-guided search*, *partial restart*, and *packaging* so that the agent cannot skip hardware grounding, cannot silently overwrite failed attempts, and always leaves an auditable path from the user's task to the submitted kernel artifact. The seven numbered boxes in Figure 5 define the outer workflow.

① **User input.** The user supplies the platform, framework or target DSL, and a kernel demo. Keeping this interface narrow is intentional: the agent receives a concrete operator target rather than a broad

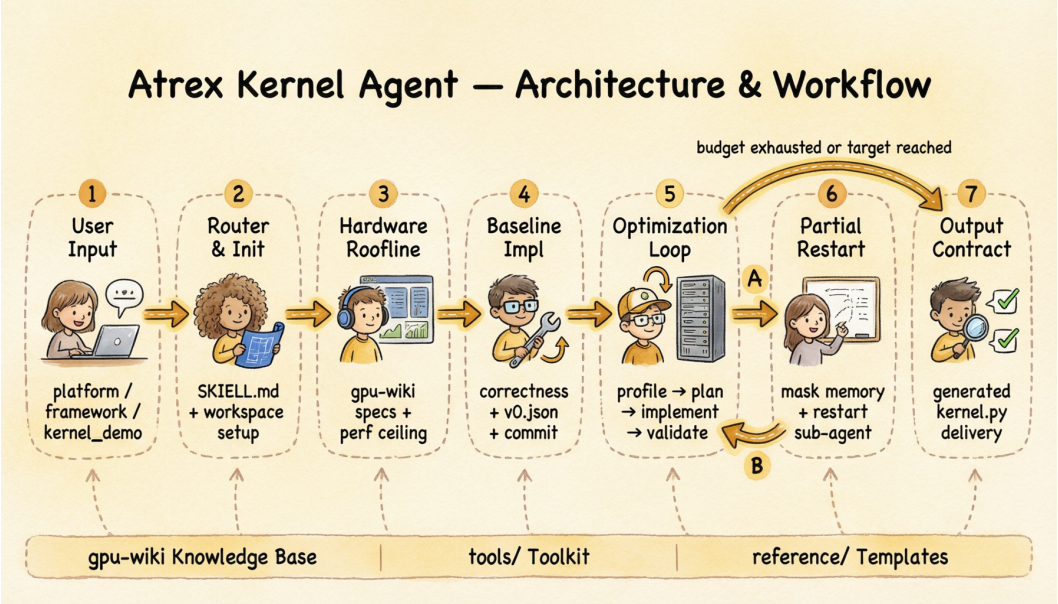

Figure 5: AKA architecture and outer workflow: the seven numbered stages from user input to evaluator-ready output, over shared resources (GPU Wiki, profiling and measurement tools, reference templates).

instruction to "optimize code," which makes subsequent hardware lookup, harness construction, and validation easier to scope to a single deployable kernel.

② **Router and initialization.** The top-level router parses the request, selects the relevant workflow components, creates an isolated workspace, and records the task configuration, assumptions, and stop conditions in the run state. This step gives the run a stable artifact boundary: later agents must update the recorded state rather than relying on conversation-only memory.

③ **Hardware Roofline.** Before generating a kernel, the router queries GPU Wiki for sourced hardware specifications, computes FLOPs, bytes moved, arithmetic intensity, bound type, and the relevant Roofline ceiling, and archives the source path for every hardware value. This grounding prevents two common failure modes: optimizing for the wrong bottleneck and inventing peak throughput or bandwidth numbers that make performance claims unverifiable.

④ **Baseline implementation.** The baseline component builds the first correct target-DSL implementation and its test harness, measures baseline latency and utilization, and initializes the run memory. The baseline is deliberately correctness-first: it establishes a runnable kernel and a rollback point before performance search starts.

⑤ **Optimization loop.** The profile optimizer runs the inner loop expanded in Figure 6: profile, extract bottlenecks, query knowledge, plan, apply one optimization category, validate, record memory, and check whether to stop. Making optimization a loop rather than a one-shot rewrite lets the agent attach each edit to profiler evidence and measure whether the edit actually helped.

⑥ **Partial restart.** When the optimizer concludes that no actionable optimization direction remains, the partial-restart path masks a subset of iteration memories while preserving the baseline, latest accepted kernel, and full audit trail, then starts a fresh sub-agent from the remaining state. The partial view prevents prior failed hypotheses from anchoring the new agent's judgment, allowing it to reassess the kernel and identify opportunities that the previous search considered exhausted. This is a *dropout-style partial restart*: it drops selected search memories, not accepted code or measured evidence, to help the optimizer escape a local optimum.

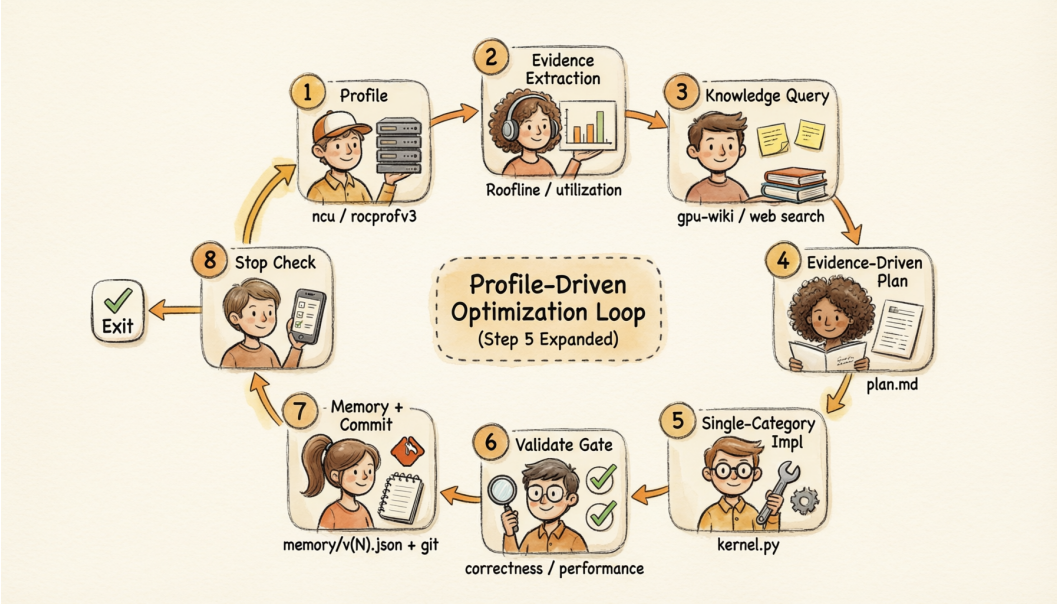

Figure 6: Profile-driven optimization loop inside AKA: the eight numbered stages that turn profiler evidence into one scoped, validated implementation change per iteration.

⑦ **Output contract.** The packaging component converts the accepted implementation into a single evaluator-ready kernel artifact. Tests, logs, notebooks, profiles, and external file dependencies are excluded, so the final artifact is deployable code rather than a workspace snapshot.

Execution components. The system comprises five components under the router: the baseline implementer, bottleneck-analysis helper, profile optimizer, partial restart handler, and output-contract packager. Their separation is a control mechanism, not merely an implementation convenience. Hardware reasoning stays in the bottleneck helper, source-code edits stay in the implementer / optimizer, recovery is explicit rather than implicit, and packaging is isolated from experimentation so that temporary files cannot leak into the submitted artifact.

GPU Wiki knowledge base. The local knowledge base has two parts. *Reference kernels*: **298** reference kernels organized by vendor architecture (**115** NVIDIA, **142** AMD, **41** architecture-agnostic), which the agent can inspect or adapt. *Documents*: **244** structured optimization-knowledge documents, indexed by a relationship graph and organized into five categories: optimization patterns (87; vendor-agnostic theory plus AMD- and NVIDIA-specific details), framework/profiler/ISA references (109), DSL conversion recipes (27), pitfall records (16), and hardware-spec tables (3). Hardware-spec values used in a run must be sourced from GPU Wiki and archived with a path citation; unsourced compute peaks, bandwidths, occupancy limits, or cache/LDS capacities invalidate the run.

Tools and external references. The workflow also ships profiling and measurement helpers for official-profiler data collection, kernel timing, utilization analysis, and bandwidth-ceiling measurement. Beyond the local knowledge base, the workflow can cache upstream reference projects (e.g., CUTLASS / CuTeDSL, FlyDSL, Triton, AITER, FlashInfer, and FlashMLA) for source-level API and ISA lookup. Public web lookup is a last resort when the local Wiki and reference projects are silent on a low-level detail.

5.3 Profile-Driven Optimization Loop

The outer workflow enters the optimization loop only after a hardware Roofline estimate and a correct baseline exist. Figure 6 expands Step 5 of Figure 5 into eight ordered stages. The order matters: each iteration starts from measurement, turns measurement into a hypothesis, maps the hypothesis to a documented optimization tactic, changes one class of code, and records the outcome before deciding whether another iteration is justified.

The eight stages are:

① **Profile.** The loop profiles the current kernel with the official hardware profiler—`ncu` on NVIDIA or `rocprofv3`/ATT/PMC/assembly on AMD—rather than using latency alone. Timers still determine whether a change is faster, but profiler counters determine what kind of bottleneck the next edit should target.

② **Evidence extraction.** The bottleneck helper converts raw counters into Roofline and utilization evidence: achieved bandwidth or compute, occupancy, memory transactions, wave / warp behavior, instruction mix, and whether the observed limit matches the semantic bound computed in the outer workflow. The output is a concrete bottleneck hypothesis, not a generic request for speedup.

③ **Knowledge query.** The agent retrieves the relevant GPU Wiki notes, hardware-spec entries, pitfalls, reference kernels, and local reference-project source. Public web lookup is allowed only when the local knowledge base and cached projects are silent. This step keeps optimization tactics grounded in documented hardware and library behavior.

④ **Evidence-driven plan.** The agent writes an explicit plan: the measured bottleneck, the knowledge sources it used, the expected performance effect, the correctness risks, and the single optimization category to try next. Requiring an explicit plan forces the model to connect evidence to action before editing code.

⑤ **Single-category implementation.** The agent edits the candidate kernel in one category at a time: tiling, vectorization, memory layout, prefetching, synchronization, split / fusion structure, or instruction selection. This constraint trades off search speed for attribution: when performance changes, the log can identify which class of edit caused it.

⑥ **Validate gate.** Correctness is checked before performance. A kernel that fails correctness is rejected immediately; a correct kernel is timed under the same harness and compared with the previous accepted state. Regressions are reverted unless they are explicitly kept as a measured trade-off toward a later plan.

⑦ **Memory update.** Accepted iterations update the structured run memory and running summary; rejected attempts are recorded with the evidence and failure reason. This separates search from memory: later iterations reason over structured records instead of relying on hidden conversation state.

⑧ **Stop check.** The loop does not stop by a fixed external rule such as a hard target or exhausted budget. Instead, the agent inspects the current measurement history, accepted and rejected edits, and unmasked memory, then decides whether it has achieved the objective well enough or whether no actionable optimization direction remains. In the latter case, control returns to the outer partial-restart path (Figure 5), which masks selected memories before a fresh sub-agent reassesses the remaining optimization space.

This artifact boundary is what makes the loop more than repeated prompting. Each iteration must turn profiler evidence into a concrete bottleneck hypothesis, retrieve the relevant GPU Wiki notes or reference-project source, write an explicit plan, and change exactly one optimization category before validation. The resulting log gives the case studies below a causal trace: not just that the final kernel is faster, but which evidence led to which edit and which edits were kept or reverted.

In the evaluation below (§5.4), the *vanilla* condition uses the standard one-pass FlyDSL prompt (§4.1); the *AKA* condition runs the same base model inside this workflow. Everything else is held fixed: base model, target DSL, evaluation contract, and the hidden-information policy of §4.

5.4 Optimizer-Augmented Evaluation: Setup

Scope. This is a controlled case study, not a benchmark-wide ranking. We pair two base models from the §4 panel—Claude Opus 4.7 and Qwen3.7-Max—with the two conditions, on three operators that stress the agent in different ways. By semantic arithmetic intensity all three are compute-bound (§4.5), but the bottleneck they actually hit differs: `attention_forward` is throughput-bound and can approach the matrix-engine roof, whereas `chunk_gated_delta_rule_state` (a linear-

Table 8: Optimizer-augmented evaluation on Qwen3.7-Max and Claude Opus 4.7 (one production shape per operator, XPU-A). Each cell reads vanilla → optimizer-augmented for FlyDSL share, roofline S, and speedup over the production kernel.

		vanilla → optimizer-augmented		
Model	Operator	FlyDSL	S (roofline)	vs. prod
Qwen3.7-Max	`chunk_gated_delta`	$0\% \rightarrow \sim 100\%$	$0.001 \rightarrow 0.03$	$0.03\times \rightarrow 1.20\times$
	`attention_forward`	$0\% \rightarrow 99\%$	$0.06 \rightarrow 0.40$	$0.17\times \rightarrow 1.11\times$
	`mla_decode`	$14\% \rightarrow 87\%$	$0.0003 \rightarrow 0.0035$	$0.10\times \rightarrow 1.06\times$
Claude Opus 4.7	`chunk_gated_delta`	$0\% \rightarrow \sim 100\%$	$0.001 \rightarrow 0.03$	$0.04\times \rightarrow 1.31\times$
	`attention_forward`	$\sim 100\% \rightarrow 99\%$	$0.28 \rightarrow 0.42$	$0.78\times \rightarrow 1.17\times$
	`mla_decode`	$92\% \rightarrow 92\%$	$0.0023 \rightarrow 0.0042$	$0.71\times \rightarrow 1.27\times$

attention recurrence) and `mla_decode_attention` run at small, dispatch-bound shapes where roofline achievement stays near the floor and the deployed kernel's latency is the meaningful target. Each operator uses one production-representative shape, and both conditions run on that same shape and the same XPU-A hardware. Metrics follow §4.1.

One extra signal. The optimizer-augmented condition is a loop, so it leaves an iteration log: each profiled hypothesis and its measured result. The case studies read this log to explain *why* a kernel improved—evidence the aggregate numbers cannot give.

The headline metric depends on the regime. No single number reads the same across operators. For the throughput-bound `attention_forward` we report S, the fraction of the roof. For the recurrence, where the vanilla failure is a PyTorch fallback, we report the jump in FlyDSL adoption together with the speedup. For the dispatch-bound `mla_decode_attention`, S saturates near the floor, so we report the ratio to the production kernel.

Data status. All three operators are complete in both conditions for both base models. Performance is a single timed run per (op, shape). Table 8 gives the comparison.

5.5 Main Results

The two base models expose two distinct effects of the workflow. On the weaker Qwen3.7-Max the effect is *fallback-to-target-DSL dominance*. Its vanilla kernels barely use FlyDSL—0% on the recurrence and `attention_forward`, 14% on `mla_decode`, passing by PyTorch fallback (§4.3)—while the optimizer-augmented agent writes near-100% FlyDSL kernels that overtake production (Table 8). The recurrence `chunk_gated_delta_rule_state` is the clearest case: a 0%-FlyDSL fallback roughly $29\times$ slower than production becomes a near-100%-FlyDSL kernel that beats it ($1.2\times$). On the throughput-bound `attention_forward` it gains the most in roofline terms (S $0.06 \rightarrow 0.40$, $6.7\times$ over the fallback) and edges past the hand-tuned AITER kernel ($1.11\times$); on the dispatch-bound `mla_decode` it likewise passes production ($1.06\times$). All three optimizer-augmented kernels overtake the deployed kernel, whereas all three vanilla kernels trailed it ($0.03\times$ to $0.17\times$).

On the stronger Opus 4.7 the effect is mostly *optimization*: on the two attention operators its vanilla kernels are already FlyDSL ($\sim 100\%$ on `attention_forward`, 92% on `mla_decode`), so the workflow pushes already-written kernels toward the roof—lifting `attention_forward` from $S = 0.28$ to 0.42 ($0.78\times \rightarrow 1.17\times$ production) and carrying `mla_decode` from $0.71\times$ to $1.27\times$. The recurrence is the exception: like Qwen, Opus falls back to PyTorch in the vanilla condition (0% FlyDSL), and the workflow converts it into a near-100%-FlyDSL kernel that beats production ($0.04\times \rightarrow 1.31\times$). Read together, the two models trace the same library to two complementary roles: for a weaker base model it closes the *target-DSL-dominance* gap broadly (fallback → FlyDSL), and for a stronger one it closes the residual *roofline* gap on already-written kernels while still converting the one recurrence where even it falls back—beating the hand-tuned production kernel on every operator.

5.6 Case Studies: How the Optimization Workflow Helps

The aggregate results show the workflow's effect; the iteration logs show how each improvement arises. We examine one operator per regime, and each case ends with the specific advantage it demonstrates.

5.6.1 `chunk_gated_delta_rule_state`: from fallback to beating production

This recurrence is the clearest case. In the vanilla condition, Qwen3.7-Max returns a correct module that is pure PyTorch fallback—0% FlyDSL—and, at about 2.8 ms, is roughly $29\times$ slower than the production kernel (≈ 95 μs). A base model has no learned FlyDSL template for this recurrence, so it composes framework ops instead.

The optimizer-augmented workflow retrieves a direct scaffold: the AITER FlyDSL chunk-gated-delta reference kernel, a Wiki playbook for this operator family on XPU-A, the hardware-spec sheet, and a pitfalls entry (raw vs. cumulative gates, the state layout, and the 80-CU occupancy limit). The agent adapts the scaffold into FlyDSL, then optimizes against profiles: a tile sweep up to the LDS limit, prefetch and store reordering, and padding to remove bank conflicts, reverting each regression with a logged reason. The result is a near-100% FlyDSL kernel that runs in about 79 μs, approximately $1.2\times$ faster than the production kernel. Because this small-shape recurrence is dispatch-bound, roofline achievement stays near the floor ($S \approx 0.03$), so the signal here is the target-DSL-dominance jump and the speedup rather than the fraction of the roof. `torch.compile` does not rescue the recurrence either—it stays a PyTorch composition at $\approx$3 ms, essentially the vanilla fallback—so the FlyDSL kernel is about $38\times$ faster than it as well.

The advantage is concrete. The reference kernel gave the model a way to write the recurrence in FlyDSL, and the profile loop turned a first correct version into a faster one. This is the correctness illusion of §4.3, closed in one step. Opus 4.7 shows the same conversion on this recurrence: its vanilla kernel is likewise a 0%-FlyDSL fallback, and the optimizer-augmented kernel reaches near-100% FlyDSL at $1.31\times$ production—even the stronger base model falls back here and is rescued by the same scaffold.

5.6.2 `attention_forward`: the same conversion, compute-bound

The compute-bound operator shows the same conversion, with a smaller margin over production. Vanilla Qwen3.7-Max again writes a correct but 0%-FlyDSL kernel; the optimizer-augmented agent writes a 99%-FlyDSL kernel that runs $6.7\times$ faster, raising S from 0.06 to 0.40 and edging past the hand-tuned AITER production kernel ($1.11\times$). That a generated kernel overtakes AITER here is less surprising than it first reads: on this shape—a single $65{,}556$-token sequence with 16 heads and a head dimension of 72, an awkward non-power-of-two for MFMA tiling—the general AITER varlen kernel itself reaches only $\approx 36\%$ of the roof ($S \approx 0.36$), leaving room for a shape-specialized kernel to pass it. The library's value is on the compute path: the workflow picks among its FlyDSL flash-attention references, avoids documented construction pitfalls that otherwise cause repeated compile failures, and follows the ISA targets—vectorized access, MFMA utilization, no register spills. The stronger base model sharpens the same point: Opus 4.7's vanilla kernel is already FlyDSL at $S = 0.28$, and the workflow lifts it to $S = 0.42$ at $1.17\times$ production—optimization rather than conversion, but the same lever set. The advantage here is direction: the library tells the agent which levers move a working kernel toward the roof.

5.6.3 `mla_decode_attention`: edging past hand-tuned production

The latency-bound operator is the hardest test, because its ceiling is a hand-written assembly kernel rather than a framework op. The vanilla agent stays far from that ceiling: a mostly-fallback kernel at about $0.1\times$ the production AITER time. The optimizer-augmented workflow classifies the problem as dispatch-bound and restructures the decode as a split-KV computation with an online-softmax reduction, spreading the scattered gather across compute units. After profiling-driven tuning, the resulting 87%-FlyDSL kernel reaches about 18 μs and edges past the hand-tuned AITER kernel ($1.06\times$). This is the result that most directly answers the paper's question: a generated kernel beating a hand-written production kernel on a deployed operator. The advantage here is structural reasoning—the split-KV restructuring the base model adopts only once the workflow frames the problem by its bound.

Across all three operators, the advantage is similar in kind. AKA does not hand the agent a finished kernel. It supplies the missing pieces—a regime-appropriate target, a reference scaffold, the pitfalls to avoid, the ISA-level levers, and a measurement loop—and the agent does the rest. These are the gaps §4 traced the vanilla failures to.

6 Discussion

6.1 Limitations

Trace scope and evaluation coverage. Trace collection in this release covers selected XPU-A and H20 production clusters with more than 10k deployed cards. These traces cover compute-limited, memory-rich GPU fleets, so the sampled problems represent that traced deployment slice rather than every hardware class. This draft reports empirical results only on XPU-A; broader accelerator validation remains future work and will test whether the same benchmark construction and roofline-normalized scoring remain informative across accelerator families. We do not claim that the current trace slice represents every future hardware class.

Inference-only. The current release covers inference kernels exclusively. Training workloads—in particular backward kernels and optimizer-step kernels—are out of scope for this version.

6.2 Future Work

More accelerators and workload regimes. Future releases should extend empirical evaluation beyond the current XPU-A setting to NVIDIA-side deployments and higher-throughput accelerators. This expansion is not only a hardware exercise: different accelerator classes host different model mixes, precision formats, kernel libraries, and serving or training paths, so the benchmark should grow by capturing the workload regimes that appear on those fleets. The roofline-normalized score generalizes to these settings; the main engineering work is calibrating hardware peaks and validating the reference and evaluation path per accelerator.

Periodic benchmark refresh. Production serving workloads change as models, engines, and kernel libraries evolve. We therefore plan to refresh Atrex-Bench on a regular cadence from new production traces, updating operator sets, shape distributions, and importance weights while keeping each released version frozen for reproducibility.

Scaling agentic optimization. Future versions of AKA will decompose kernels into prologue, mainloop, and epilogue regions for context-isolated sub-agent tuning, and explore multi-model planning, implementation, and review workflows. Longer campaigns of 300 or more iterations will distill validated experience back into GPU Wiki, while new templates, cross-project practices, and composable optimization primitives expand the search space. More precise retrieval and progressive disclosure will expose this knowledge incrementally as required by the search process.

7 Conclusion

We presented **Atrex-Bench**, a GPU kernel generation benchmark sourced from full-cluster production inference traces and scored with importance-weighted roofline metrics. On 30 operators and 440 shapes, six frontier coding agents reach at most $\sim 10\%$ of the hardware roofline—with the residual gap concentrated in domain-knowledge-intensive patterns rather than raw coding ability. Motivated by this finding, we co-released **AKA**—a profile-driven kernel-optimization agent that combines iterative measure–revise search, optimization dropout for escaping stalled search contexts, and a layered knowledge base of expert experience, reference kernels, and upstream open-source practices. A controlled case study shows that the agent converts PyTorch fallbacks into real FlyDSL kernels that match or exceed hand-tuned production baselines. Both artifacts are open-source; we hope they provide a deployment-aligned evaluation signal and a reusable optimization agent that lowers the barrier to production-relevant progress in LLM kernel generation.

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A Per-Operator Results

This appendix expands the operator-balanced aggregates of §4 into per-operator and per-model detail. All numbers come from the same evaluation run as the main text—six candidates, 30 operators, 440 shapes, XPU-A—with the metrics defined in §4.1.

The production-weighted score is set by a few heavy, low-achievement operators. Table 9 lists every operator with its roofline regime, median semantic arithmetic intensity across its shapes, production importance weight w_i, shape count, mean shape-pass rate across the six models (the model-independent difficulty of §4.4), and the per-operator achievement S_i of the two strongest backends. Two facts drive S_{agg}. First, importance is concentrated: the five heaviest operators hold 63.7% of weighted production wall-time, and `unified_attention` alone holds 36.1%. Second, those heavy operators are exactly the ones no model reaches—`unified_attention` tops out at $S = 0.07$ (GPT-5.5) and 0.01 (Opus 4.7), `fused_moe` at 0.22, `block_scaled_mm` at 0.21—while several light bandwidth-bound operators clear $S > 0.3$ (`moe_sum_reduce` 0.59, `l2_norm` 0.44). Weighting by w_i therefore pulls the aggregate down to $\sim$0.11 and localizes the Opus–GPT split of §4.2: the two are even on the easy operators, but GPT-5.5 is the only model with non-trivial S on the heavy compute-bound ones (`unified_attention` 0.07 vs. 0.01; `fused_moe` 0.22 vs. unmeasured, as Opus passes it only by a non-DSL fallback). The difficulty column reads the suite from the other direction: the hardest operators are uniformly low-precision fused or matrix-engine kernels (`fp8_blockscale_fused_moe` 22.2%, `fused_rmsnorm_quant` 34.8%, `per_token_group_quant_fp8` 44.7%, `attention_forward` 45.2%), while nine elementwise and normalization operators are solved by every model.

Where each model breaks. Table 10 partitions the 683 failing units by model and stage. This breakdown tracks generation quality and, more usefully, the *kind* of failure. The two weakest backends account for 68% of all failures and fail mostly at compile time: GLM-5.1 alone contributes 288, dominated by 152 candidates that raise before producing an artifact, 61 compile timeouts, and 19 that are not even valid `nn.Modules`; DeepSeek-V4-Pro adds 175 failures (mostly compile and numeric failures, plus 26 runtime timeouts). The three strongest fail differently. GPT-5.5 fails almost entirely on numeric mismatches (28 of 30 units). Opus 4.7's 46 failures are unique in the panel: half (23) are *correct-but-slow*—kernels that pass numerics but miss the performance budget—rather than the compile or numeric breakage that dominates the weaker models. The soft, performance-side failure is thus a signature of the strongest backend, consistent with the residual-roofline-gap reading of §4.2.

Table 9: All 30 operators, sorted by importance weight w_i. AI is the median per-shape arithmetic intensity in FLOP/byte; Regime is its class (comp/mem/idx; "–" for pure-indexing); Pass is the mean shape-pass across the six models; S_{Opus}, S_{GPT} are the per-operator median S of the two leaders.

Operator	Regime	AI	w_i (%)	#sh	Pass (%)	S_{Opus}	S_{GPT}
`unified_attention`	comp	112	36.1	25	69.3	0.01	0.07
`fused_moe`	comp	415	10.4	23	100.0	–	0.22
`block_scaled_mm`	comp	823	8.5	24	56.9	0.16	0.21
`fp8_blockscale_fused_moe`	comp	121	4.7	6	22.2	–	0.02
`paged_attention_decode`	mem	2.6	4.0	8	66.7	0.02	0.02
`reshape_and_cache`	idx	–	4.0	8	100.0	0.23	0.32
`topk_filter`	idx	–	3.2	8	83.3	0.03	0.01
`gated_delta_rule_update`	comp	90	3.2	17	57.8	0.01	0.01
`fused_qkv_rope`	mem	0.7	3.1	6	100.0	0.00	0.00
`rms_norm`	mem	0.8	2.5	56	83.3	0.17	0.07
`mla_decode_attention`	comp	34	2.1	3	83.3	0.00	0.01
`attention_forward`	comp	4068	2.0	21	45.2	0.16	0.14
`causal_conv1d`	mem	3.0	2.0	9	81.5	0.07	0.07
`moe_topk_gating_softmax`	mem	0.9	1.9	10	91.7	0.01	0.01
`fused_qk_rmsnorm`	mem	0.6	1.7	4	100.0	0.00	0.00
`silu_and_mul`	mem	0.8	1.6	37	100.0	0.27	0.25
`chunk_gated_delta_rule_state`	comp	45	1.4	25	67.3	0.00	0.00
`fused_add_rms_norm`	mem	0.5	1.0	19	83.3	0.30	0.21
`moe_align_block_size`	idx	–	1.0	6	100.0	0.00	0.00
`mrope`	mem	0.6	0.9	5	83.3	0.27	0.23
`chunk_delta_rule_output`	comp	51	0.8	16	50.0	0.01	–
`fp8_dynamic_per_token_quant`	mem	0.3	0.8	20	70.0	0.25	0.16
`linear_sigmoid_mul`	comp	1018	0.7	9	57.4	0.52	0.45
`per_token_group_quant_fp8`	mem	0.3	0.5	19	44.7	0.39	0.15
`gated_rms_norm`	mem	1.3	0.4	7	100.0	0.34	0.29
`l2_norm`	mem	0.8	0.4	13	100.0	0.44	0.41
`moe_count_and_sort`	idx	–	0.4	5	86.7	0.00	0.00
`fused_rmsnorm_quant`	mem	0.7	0.3	11	34.8	0.03	0.13
`moe_sum_reduce`	mem	0.4	0.3	7	100.0	0.59	0.43
`layer_norm`	mem	1.7	0.1	13	70.5	0.14	0.14

Table 10: Failure taxonomy by model over the 683 failing units (counts, not operator-balanced). Compile: exception before artifact (exc), timeout/OOM (t/o), or `Model` not `nn.Module` (struct). Runtime: numeric mismatch, timeout (t/o), exception (exc). Perf: correct but over budget (slow).

	Compile			Runtime			Perf	
Model	exc	t/o	struct	numeric	t/o	exc	slow	Total
Claude Opus 4.7	1	0	0	20	0	2	23	46
GPT-5.5	0	0	0	28	0	2	0	30
Qwen3.7-Max	18	0	0	48	0	2	0	68
Kimi-K2.6	20	21	0	33	0	2	0	76
GLM-5.1	152	61	19	55	0	1	0	288
DeepSeek-V4-Pro	70	3	0	73	26	2	1	175
Total	261	85	19	257	26	11	24	683